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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/971,949	10/05/2001	Joseph H. End III	TN205	4081

7590 07/13/2005

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EXAMINER	
NGO, CHUONG D	

ART UNIT	PAPER NUMBER
2193	

DATE MAILED: 07/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/971,949	END, JOSEPH H.	
	Examiner	Art Unit	
	Chuong D. Ngo	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 April 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-14 stand rejected under 35 U.S.C. 102(b) as being clearly anticipated by Tate et al. (3,733,477).

Tate et al. discloses in figure 1 a circuit for calculating and outputting a modulo value (the final partial remainder) including a plurality of subtraction circuits (24,26,28) for subtracting a common dividend signal (22) from test values signals (50,52,54,56,58,60,62) each representing a respective integer multiple of the divisor to produce remainder signals (66,68,70), a logic (158,160,162, see figure 3) for determining which of the remainder signals represents a true remainder, and a multiplexer (150,152,154,156, figure 3) for outputting the true remainder as claimed.

As per claims 8 and 13, the recitation that the dividend has a value ranging form 0 to 65535, and the devisor comprise a fixed value of 9973 is merely an intended field of used, the circuit of Tate et al is clearly capable of operating on these values.

As per claims 10 and 11, the subtract circuits as in figure 1 clearly receiving the test value signals before or substantially simultaneously with the dividend signal as the test value signals passing through two registers and a logic gate while the dividend passing through three registers

2. Claims stand rejected under 35 U.S.C. 102(b) as being clearly anticipated by Yoshida (5,638,314).

Yoshida discloses in figure 1 a circuit for calculating and outputting a modulo value (the final partial remainder) including a plurality of subtraction circuits (3) for subtracting a common dividend signal from test values signals (outputs from 4) each representing a respective integer

multiple of the divisor to produce remainder signals, a logic (8) for determining which of the remainder signals represents a true remainder, and a multiplexer (7) for outputting the true remainder as claimed.

As per claims 8,10,11 and 13, the recitation that the dividend has a value ranging form 0 to 65535, and the divisor comprise a fixed value of 9973 is merely an intended field of used, the circuit of Yoshida is clearly capable of operating on these values. In addition, as the circuit is set with a constants divisor, the subtract circuits 1 clearly receiving the test value signals before or substantially simultaneously with the dividend signal.

3. Applicant's arguments filed on 04/11/2005 have been fully considered but they are not persuasive.

It is respectfully submitted that both Tate and Yoshida disclose the circuit for perform a division on any values of a dividend and divisor including those recited in claims 8 and 13, and it is clear from figures 1 of Tate and Yoshida that for those dividend and divisor that the dividend is not greater than 7 times divisor, as those recited in 8 and 13, the selected result of the subtractions would be the final remainder as claimed. Further, it is respecfully submitted that the test value signal in Tate and Yoshida can be seen as being hard coded in the circuit when the divisor is keep constant.

4. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

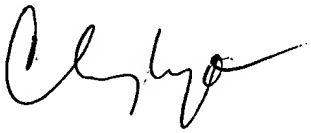
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

5. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chuong D. Ngo whose telephone number is (571) 272-3731. The examiner can normally be reached on Tuesday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kakali Chaki can be reached on (571) 272-3719. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Chuong D Ngo
Primary Examiner
Art Unit 2193

07/08/2005